Low-Cost Flip-Chip Alternatives for Millimeter Wave Applications

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Abstract **— This paper discusses alternative flip-chip approaches in the millimeter wave frequency range. In comparison to common stud bumping or gold plating techniques at these frequencies this contribution deals with bump formation by micro balls and conductive adhesives (polymeric bumps). In the latter process special bump shaping is supported by introducing an additional photo resist process. The photoresist also serves as an underfill for the flip-chipped device. Utilizing these bumping techniques flip-chipped test systems in coplanar waveguide (CPW) design were fabricated and then characterized via S-parameter measurements at W-band.**

I. Introduction

Due to the advances in semiconductor technology a wide variety of monolithic millimeterwave integrated cicuits (MMIC) is readily available for a powerful and flexible system design up to W-band frequencies. Cost effective, reliable, and reproducible packaging is the key issue for the development of millimeter wave systems. For multichip modul (MCM) assembly the flip-chip approach is one of the most promising [1–3]. Here, the conventional wire bonds are replaced by metal or conductive polymeric bumps fabricated on either the chip or the substrate. The bumps provide a means of both chip attachment and electrical interconnection to the carrier. Fig. 1 shows the chip mounted upside down on the substrate. In comparison to wire bonding flip chip technology offers improved electrical performance of the interconnect [3, 4] and allows higher packaging density [4, 5]. Along with the CPW design it reduces fabrication and assembly costs [3, 4]. Before alternative bump forming techniques suitable for further cost reduction are discussed the next section summarizes important design parameters of flip-chip interconnects. Finally, first experiments are reported.

II. Design Parameters for Flip Chip Interconnects

This section describes a set of parameters that is important for the design of flip-chip interconnects using CPW technology in the W-band. The air gap between

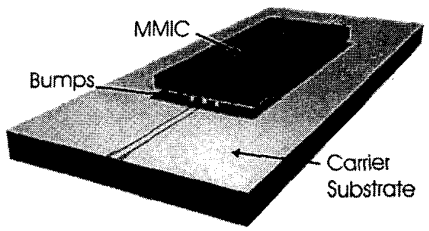

Fig. 1. Flip chip configuration in CPW technology.

carrier substrate and chip should be large enough to avoid detuning effects. Fig. 2 shows the simulated return and insertion loss of a 50 Ω CPW test structure on alumina substrates. Here, an interruption of the CPW on the carrier is bridged by a CPW test chip connected via six metallic bumps. The results demonstrate the need for a minimum gap of 20 μm at 76.5 GHz.

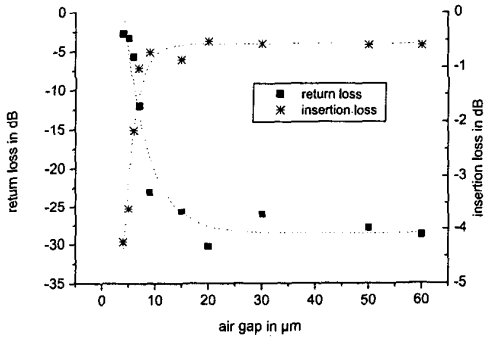

Fig. 2. Simulated return and insertion loss as a function of the air gap.

Also the bump properties themselves have to be taken into account. Mimimum reflections can be achieved by altering the bump shape [4] or stagger-

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ing the bumps and introducing short circuit bridges between the ground bumps [6,7]. The overlap between the lines on the chip and the substrate should be minimum and, thus, is determined by the diameter of the bumps [1]. Other important design criteria like the influence of backside metallization, underfill, and the number of ground bumps are well known and discussed e.g. in [1,5]. Table I summarizes the deduced parameters for the 50 Ω test system. The fabricated test chips were comparable in size with commercially available MMIC. Pad dimensions and pitch were chosen accordingly. The chips were mounted using three different bump forming techniques to be described in the following.

TABLE I. Design table for the CPW test systems at 76.5 GHz.

Parameter	Value
air gap	20 μm-100 μm
substrate thickness	254 μm
test chip thickness	127 μm
bump diameter	< 50 μm
bump shape	cylindrical, square, rectangular
overlap	50 μm
ground-to-ground spacing on substrate	100 μm
line width on substrate	50 μm
ground-to-ground spacing on chip	78 μm
line width on chip	38 μm
dielectric constant	9.8
backside metallization	no
under-chip metallization	no

III. Applied Bump Techniques

The bumps and the complete test systems were assembled using pick and place utilities with a split field optic for highly accurate placement (± 4 μm) and a heated chuck for simultaneously curing epoxies. Furthermore, both a ball and a wedge bonder were available for bump creation purposes.

A. Polymeric bumps

The polymeric bumps are fabricated by applying the pin-tranfer-technique. The bump height and diameter mainly depend on the diameter of the tip of the stamp and the thickness of the adhesive film. Using a single component, solvent free, silver filled epoxy a curing temperature of only 150 degree Celsius is possible. With a 30 μm tip diameter and an epoxy film of estimated 20 μm thickness the bumps are approximately 40 μm in diameter and up to 15 μm in height.

For more precise bump forming a modified technique is proposed. In a first step photo resist is spin coated onto the carrier substrate. As in the electroplating process [4,8], bump location and shape are then defined in a photolithographic step leaving small buckets for the bumps. The latter are realized in the next step by filling the buckets with conductive epoxy either by stamping as described above or by dropping. Curing the epoxy next also hardens the photoresist which then serves as chip support and stress reducer. Fig. 3 offers a bird's view of the photoresist on the carrier substrate, here with rectangular bumps. The slight misalignment of the bumps (approx. 15 μm) is caused by poor adhesion due to the small width-to-height ratio of the strip. This can easily be circumvented by widening the strip in uncritical areas.

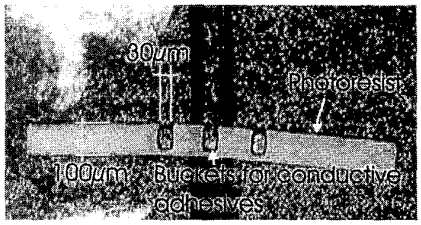

Fig. 3. Photoresist SU-8 test strip for bump forming and ship support.

Because the photoresist is kept for chip support it should guarantee good adhesion, sufficient film uniformity, firmness, chemical resistance, and adequate thermal characteristics. Suitable thick photo resists are well known from applications like in micromechnical devices. In the experiments described here SU-8 [9] proved to be appropriate. Table II summarizes a set of suitable parameters for the photoresist process as applied above.

B. Microball bumps

A different approach to get compliant bumps is to use uniform, pre-manufactured gold balls that are then either soldered or epoxied onto the substrate. The chip is attached to the balls either by a standard thermocompression bonding process or, as in our simple experiments and for demonstration purposes, with conductive adhesive. Here, the microballs were extracted by vacuum suction from commercially available gold powders [10] with a mean particle diameter of 44 μm and 38.7 μm, respectively. Fig. 4 depicts three 40 μm

TABLE II. Applied process for the SU-8 50 test strip.

Process step	Parameter
spin coating	900 rpm, 10 sec
relaxation time	5 min
pre-soft bake	5 min @ 50 °C
soft bake	30 min @ 95 °C
exposure time	20 sec @ 400 nm - 450 nm
pre-post bake	5 min @ 50 °C
post bake	15 min @ 95 °C
relaxation time	5 min
development	5 min in propylene-glycol-methyl-ether-acetate

microballs attached to a test substrate using isotropic conductive adhesive. The position of the microballs on top of the epoxy drops is not very stable, though, which leads to the observed misalignement. For more precise positioning circular holes can be etched into the carrier metallization so as to catch the balls in the desired place. Alternatively, the microballs could be mounted by thermocompression bonding. Sophisticated equipment with state-of-the-art positioning gears is readily available for this purpose in an industrial environment and would require only little modification.

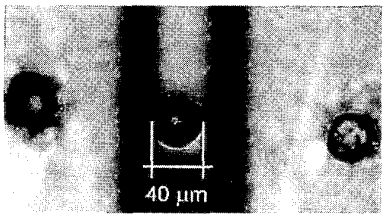

Fig. 4. Three 40 μm micro-balls attached to a test substrate using isotropic conductive adhesive.

C. Stud bumps

For comparison, finally, stud bumps were produced using the common altered ball bonding process, where the gold wire is cut after the first bump has been set [8]. To control the quality of the manually produced bumps these were flattened before actually mounting the test chip. Fig. 5 shows the histogram of the height and the diameter of 27 produced bumps and how they are correlated. The reproducibility appears to be quite satisfying but, because of the available ball bonder (bond wire diameter of 60 μm), the bumps turn out to be slightly too big. As matter of illustration Fig. 6 shows three stud bumps that were used in the subsequent experiments.

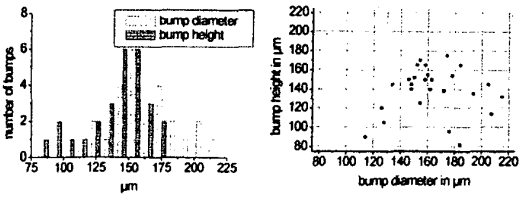

Fig. 5. Histogram of the height and the diameter of the stud bumps and its correlation.

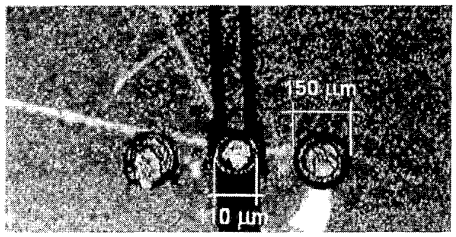

Fig. 6. Three stud bumps attached to a test substrate with a ball bonder (flattened to a height of 100 μm).

IV. CPW Test System and Measurements

The gold plated alumina substrates were structured and shaped employing photolithography and laser material processing, respectively. The test chips were mounted on the carrier substrate by applying the different flip-chip approaches described above.

The test systems were characterized by means of vector network analysis (VNA) and Cascade Microtech Probe Station with W-band CPW probes (pitch: 125 μm). The available measurement equipment only allowed a one-port-two-path calibration process using a standard calibration substrate.

The measured transmission and reflection characteristics in the design frequency range are presented in Fig. 7. Results for the CPW through connection, i.e. without flip-chipped device, are shown for reference. In comparison to the reference line the input reflection is slightly increased. This explains the higher transmission loss of both the polymeric and the stud bumps. The microball bumps, however, exhibit excess loss that varies significantly across the frequency range. This hints at a poor connection quality that is most likely related to the simplicity of the positioning process used here. In the design frequency range the flip-chip approach using polymeric bumps compares well with the stud bump test system, both providing a low-loss interconnect. To ascertain these findings further measurements were conducted later on in the upper W-band.

The results depicted in Fig. 8 confirm the previous observations and, in particular, the poor performance of the microball bonds. Closer investigations revealed the deterioration of this test system with time, eventually leading to a complete failure. While more effort is needed here to improve the technology, the polymeric bump formation seems to be quite competitive.

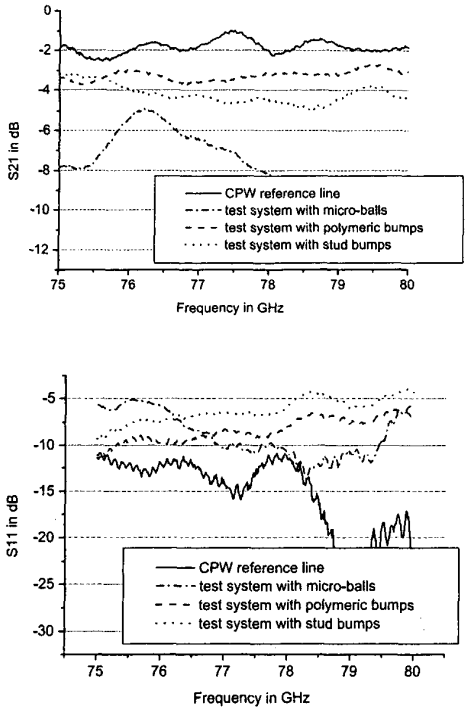

Fig. 7. Measured transmission and reflection of flip-chip test systems and CPW reference line without flip-chipped test chip in the desired frequency range.

V. Conclusion

In this contribution alternative solutions to the established flip chip interconnects for millimeter wave applications were proposed. Flip chip interconnects based on microballs and conductive adhesives with bump forming capability offered by the additional usage of photo resist were presented. Flip chip test systems were fabricated and measured at W-band. The microball approach is very appealing because of its intrinsic simplicity but further efforts have to be undertaken to improve the reliability. The functionality of the polymeric bump process is fully validated by the

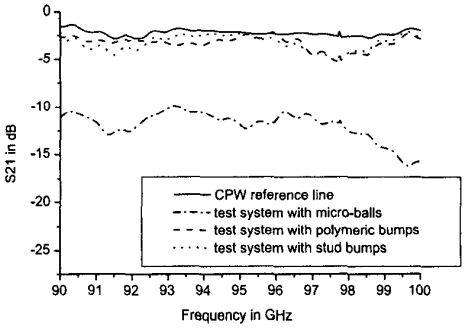

Fig. 8. Measured transmission of flip-chip test systems and CPW reference line without flip-chipped test chip in the upper W-band.

measurement results. These approaches offer the realization of flip-chip configurations with standard equipment for MCM assembly at low cost in comparison to industrial flip-chip bonding tools.

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